



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

TM

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/622,408	07/18/2003	Kee Park	5646-58IPCT2	4182
20792	7590	03/01/2004		EXAMINER
MYERS BIGEL SIBLEY & SAJOVEC PO BOX 37428 RALEIGH, NC 27627			AUDUONG, GENE NGHIA	
			ART UNIT	PAPER NUMBER
			2818	

DATE MAILED: 03/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/622,408	PARK ET AL.	
	Examiner Gene N Aduong	Art Unit 2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on ____.
- 2a) This action is **FINAL**. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 30-34 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) Claim(s) ____ is/are allowed.
- 6) Claim(s) 30-34 is/are rejected.
- 7) Claim(s) ____ is/are objected to.
- 8) Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on ____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. ____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. ____
3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date <u>071803</u> .	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
	6) <input type="checkbox"/> Other: ____

DETAILED ACTION

Information Disclosure Statement

1. This office acknowledges receipt of the following items from the applicant:
 - Information Disclosure Statement (IDS), filed on July 18, 2003.
 - Preliminary Amendments filed July 18, 2003.
 - Claims 1-29 and 35-64 had been canceled.

Specification

2. The disclosure is objected to because of the following informalities: The cross-reference to related Application Serial No. is missing.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 30-34 are rejected under 35 U.S.C. 102(e) as being anticipated by Gillingham et al. (Pub No. US 2003/0123269 A1).

Regarding claim 30, Gillingham et al. disclose a content addressable memory (CAM) array (Figures 2-4), comprising: a first match line segment associated with a first row of CAM cells (cells 104) in the CAM array; an inverter (inverter 210) having an input electrically coupled to the first match line segment, and a match line precharge support circuit (match line circuits

220, 212) comprising a first PMOS transistor having a gate terminal electrically coupled to an output of the inverter (figures 2-3), a first current carrying terminal that is electrically coupled to the first match line segment and a second current carrying terminal that is electrically coupled to a power supply line (figures 2-4).

Regarding claim 31, Gillingham et al. disclose the CAM array of claim 30, wherein the match line precharge support circuit further comprises: a second normally-on PMOS transistor (figure 3a, PMOS P2) having a first current carrying terminal that is electrically connected to the second current carrying terminal of the first PMOS transistor and a second current carrying terminal that is electrically connected to the power supply line (figure 3a).

Regarding claim 32, Gillingham et al. disclose the CAM array of claim 30, wherein the match line precharge support circuit further comprises: a second normally-on PMOS transistor having a first current carrying terminal that is electrically connected to the first match line segment and a second current carrying terminal that is electrically connected to the first current carrying terminal of the first PMOS transistor (figure 3a).

Regarding claim 33, Gillingham et al. disclose the CAM array of claim 31, wherein the second normally-on PMOS transistor has a gate terminal that is responsive to a P-bias voltage having a magnitude sufficient to maintain the second normally-on PMOS transistor in a linear mode of operation (figure 3a, PMOS transistor has a gate terminal that is responsive to ground potential to maintain the normally on PMOS transistor in a linear mode of operation).

Regarding claim 34, Gillingham et al. disclose the CAM array of claim 30, wherein a pull-down path of the inverter comprises: a first NMOS pull-down transistor having a gate terminal that is electrically connected to the input of the inverter and a drain that is electrically

connected to the output of the inverter; and a second NMOS pull-down transistor having a gate terminal that is responsive to an N-bias voltage having a magnitude sufficient to maintain the second NMOS pull-down transistor in a linear mode of operation, a drain that is electrically connected to a source of the first NMOS pull-down transistor and a source that is electrically connected to a reference supply line (figure 2b, page 4, paragraph [0045]+).

Conclusion

5. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

GA
February 10, 2004



Gene N Aduong
Primary Examiner
Art Unit 2818